REMARKS

Favorable reconsideration of this application in light of the above amendments and the following remarks is respectfully requested.

Claims 1-15 are pending within this application. Claims 4 and 11 are amended herein. No claims have been allowed.

Claim Rejections - 35 U.S.C. § 102

The Examiner has rejected 1, 3-4, 6-8, 10-11 and 13-15 under 35 U.S.C. § 102(e) as being anticipated by Somekh (U.S. Patent No. 6,292,334).

In response in a first instance, applicant has amended dependent claim 4 and amended dependent claim 11 to incorporate therein limitations from independent claim 1 and independent claim 8, to thus provide amended claim 4 and amended claim 11 as additional independent claims.

In response in a second instance, applicant respectfully disagrees in part with the Examiner's reading of Somekh insofar as the Examiner asserts at page 2, last clause of the office action mailed 14 January 2003 that Somekh's reference numeral 14 corresponds with a patterned first dielectric layer within a dual damascene structure. Rather Somekh at col. 3, last full paragraph clearly designates Somekh's reference numeral 14 as corresponding with a low k etch stop layer (i.e., a patterned hard mask layer) within a dual damascene structure. In addition, Somekh at col. 3, last full paragraph clearly also designates Somekh's reference numeral 10 as a first dielectric layer which is a blanket first dielectric layer within a dual damascene structure, rather than a patterned first dielectric layer within a dual damascene structure, as disclosed and

Thus, since each and every limitation within applicant's invention as disclosed and claimed within claim 1, amended claim 4, claim 8 and amended claim 11 is not disclosed within Somekh, in particular with respect to a first dielectric layer within a dual damascene method being formed as a patterned first dielectric layer, applicant asserts that claim 1, amended claim 4, claim 8 and amended claim 11 may not properly be rejected under 35 U.S.C. § 102(e) as being unpatentable over Somekh. MPEP 2142, 2143.03.

Since all remaining claims within the foregoing rejections are dependent upon claim 1 or claim 8 and carry all of the limitations of claim 1 or claim 8, applicant additionally asserts that those remaining claims may also not properly be rejected under 35 U.S.C. § 102(e) as being unpatentable over Somekh.

In response in a third instance, and as an adjunct with respect to amended claim 4 and amended claim 11, applicant notes that applicant specifically claims therein absence of an extrinsic hard mask layer interposed between applicant's patterned first dielectric layer and blanket second dielectric layer. In contrast, Somekh (abstract) specifically discloses and includes a patterned hard mask layer 14 interposed between Somekh's blanket first dielectric layer 10 and blanket second dielectric layer 18. For this additional reason, applicant further asserts that each and every limitation within applicant's invention as disclosed and claimed within amended claim 4 and amended claim 11 is not disclosed within Somekh.

In light of the foregoing responses, applicant respectfully requests that the Examiner's rejections of claims 1, 3-4, 6-8, 10-11 and 13-15 under 35 U.S.C. § 102(e) as being unpatentable over Somekh be withdrawn.

Claim Rejections -- 35 U.S.C. § 103

The Examiner has rejected claims 2, 5, 9 and 12 under 35 U.S.C. § 103(a) as being unpatentable over Somekh in view of Yu et al. (U.S. Patent No. 6,004,883; hereinafter "Yu").

In response, while not precluding the existence of independent patentable distinctions between: (1) Somekh in view of Yu; and (2) that which is claimed within claims 2, 5, 9 and 12, applicant predicates patentability of claims 2, 5, 9 and 12 upon their dependence upon claim 1 or claim 8.

Other Considerations

The Examiner has newly cited no additional prior art of record not employed in rejecting applicant's claims to applicant's invention.

The Commissioner is hereby authorized to charge Deposit Account No. 50-0484 the fee due as a result of this amendment and response.

SUMMARY

Applicant's invention as disclosed and claimed within claim 1, amended claim 4, claim 8 and amended claim 11 is directed towards a dual damascene method for: (1) forming an aperture through a dielectric layer; and (2) subsequently forming a patterned conductor layer within the aperture. The dual damascene method employs a patterned first dielectric layer having formed thereupon a blanket second dielectric layer, absent an extrinsic etch stop layer formed interposed between the patterned first dielectric layer and the blanket second dielectric layer. Absent from the prior art of record employed in rejecting applicant's claims to applicant's

CONCLUSION

On the basis of the above amendments and remarks, reconsideration of this application, and its early allowance, are respectfully requested.

Any inquiries relating to this or earlier communications pertaining to this application may be directed to the undersigned attorney at 248-540-4040.

Respectfully submitted,

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APPENDIX

COMPLETE COPY OF THE CLAIMS

(MARKED-UP WITH CURRENT REVISIONS)

1. A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

2. The method of claim 1 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

3. The method of claim 1 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

4. (amended) [The method of claim 1 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.] A method for forming an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0, where an extrinsic hard mask layer is not formed interposed between the

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via; and

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method.

5. The method of claim 1 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

6. The method of claim 1 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

7. The method of claim 1 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

8. A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less than about 4.0;

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

9. The method of claim 8 wherein the substrate is employed within a microelectronic fabrication selected from the group consisting of integrated circuit microelectronic fabrications, ceramic substrate microelectronic fabrications, solar cell optoelectronic microelectronic fabrications, sensor image array optoelectronic microelectronic fabrications and display image array optoelectronic microelectronic fabrications.

10. The method of claim 8 wherein the patterned first dielectric layer and the blanket second dielectric layer are each formed from a separate dielectric material selected from the group consisting of spin-on-polymer (SOP) dielectric materials, spin-on-glass (SOG) dielectric materials, amorphous carbon dielectric materials, diamond like carbon dielectric materials, carbonaceous silicate glass (CSG) dielectric materials, fluorosilicate glass (FSG) dielectric materials and aerogel dielectric materials.

11. (amended) [The method of claim 8 wherein there is not formed an extrinsic hard mask layer interposed between the patterned first dielectric layer and the blanket second dielectric layer.] A method for forming a patterned conductor layer within an aperture through a dielectric layer comprising:

providing a substrate;

forming upon the substrate a patterned first dielectric layer formed of a first dielectric material having a first dielectric constant of less than about 4.0, the patterned first dielectric layer defining a via;

forming upon the patterned first dielectric layer and filling the via a blanket second dielectric layer formed of a second dielectric material having a second dielectric constant of less

forming over the blanket second dielectric layer a patterned mask layer which defines the location of a trench to be formed through the blanket second dielectric layer, where an areal dimension of the trench is greater than and at least in part overlapping an areal dimension of the via;

etching, while employing the patterned mask layer in conjunction with an anisotropic etch method, the blanket second dielectric layer to form an aperture comprising:

the trench; and

at least a portion of the via, where the patterned first dielectric layer provides an intrinsic etch stop within the anisotropic etch method; and

forming within the aperture a contiguous patterned conductor interconnect and patterned conductor stud layer.

12. The method of claim 8 wherein the patterned first dielectric layer is formed to a thickness of from about 4000 to about 10000 angstroms.

13. The method of claim 8 wherein the blanket second dielectric layer is formed to a thickness of from about 4000 to about 7000 angstroms.

14. The method of claim 8 wherein the patterned mask layer is selected from the group consisting of patterned photoresist mask layers and patterned hard mask layers.

15. The method of claim 8 wherein the contiguous patterned conductor interconnect and patterned conductor stud layer is formed within the aperture while employing a chemical